IRIS-HEP Summer 2025 Fellow Program Project Proposal

**Software development for the Inner Tracker Data Trigger and Control system (IT-DTC)**

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**Project duration:** 12 Weeks

**Proposed start date:** July 1st, 2025

# Introduction and Project Description

The Large Hadron Collider (LHC) is in a transformative phase before it enters a new High Luminosity era. Following the upgrade of the LHC, the CMS detector requires a new tracker capable of withstanding extreme conditions. The new detector system is divided into two parts, the Inner and Outer Trackers. [1]

The CMS Inner Tracker for Phase II is a complete redesign aimed at meeting the demanding conditions of the High-Luminosity LHC (HL-LHC). This new Inner Tracker will be based entirely on highly granular silicon pixel sensors, with pixel sizes reduced to $25\times100$ $m^2$, compared to the previous $150\times100$ $m^2$, and a thinner sensor profile to improve spatial resolution and reduce occupancy in high pileup environments [2,3,4]. The tracker will feature both planar and 3D silicon sensors—3D sensors in the innermost layer for enhanced radiation tolerance, and planar sensors elsewhere—ensuring robust performance under extreme radiation (up to 1.2 Grad TID and fluence of $2.3\times10^1$ neq/$cm^2$ in the innermost regions) [3,4]. The geometric acceptance will be extended up to $|\eta| = 4$, and the system will comprise 12 forward disks and a larger active area, supporting efficient tracking and vertexing even with up to 200 simultaneous proton-proton collisions per bunch crossing [3,2].

The Inner Tracker's readout electronics are built around the RD53 family of chips, developed in 65 nm CMOS technology, which offers high radiation tolerance, low noise, and advanced features like per-pixel threshold trimming, zero suppression, and on-chip data compression [5,4]. Each chip is capable of handling high hit rates and provides detailed information for each detected hit, including time-over-threshold measurements for charge calibration [5]. The modular design, with $2\times1$ and $2\times2$ chip modules, allows for efficient assembly, maintenance, and potential future upgrades [5,3].

On the data acquisition (DAQ) side, the Inner Tracker will rely on the Inner Tracker Data Trigger and Control system (IT-DTC). IT-DTC is based on the Apollo board, which is a

custom Advanced Telecommunications Computing Architecture (ATCA) blade[6]. In total, 36 IT-DTC boards will be used to handle the enormous data rates generated by the two billion pixels [6,5]. Each backend board uses commercial Zynq System-on-Chip to run the online software and two FPGAs as the main processing units. The online software is responsible for real-time configuration, calibration, and monitoring of the detector, including threshold tuning and gain calibration using internal circuits and radioactive sources [4]. Advanced data compression and zero suppression algorithms are implemented directly in the front-end chips to reduce the data volume before transmission [5]. This integrated approach ensures the Inner Tracker can deliver high-quality data with minimal latency, supporting both prompt event reconstruction and long-term detector stability in the challenging HL-LHC environment [5,7].

By the end of the summer, I aim to successfully implement and validate calibration routines within the IT-DTC Online Software, contributing to the efficient and stable operation of the CMS Inner Tracker for the HL-LHC era.

# Project timeline and deliverables:

- **Week 1-2.** Learning the IT-DTC software structure, hardware setup and basics of the IT FE modules operation. Working with the tutorials on backend and frontend operation. Outcome: a short presentation to the working group on the outlines for the summer.
- **Week 2-8.** Working on the Pixel calibration routines. Learning the SW used for the IT R&D and porting it to the IT-DTC Online SW framework. Outcome: implemented pixelAlive at first, then noiseScan and threshold Minimisation routines, depending on the group progress.
- **Week 9-12.** Testing and verification on a hardware setup. Possible deployment on a testbeam in August 2025. Outcome: tested and merged IT calibrations in the Online SW framework.

# References

[1] https://cds.cern.ch/record/2780125/files/CR2020_063.pdf

[2] [PDF] The Phase 2 upgrade of CMS Inner Tracker- CERN Indico https://indico.cern.ch/event/803258/contributions/3582853/attachments/1962394/3262057/267-Orfanelli-CMSInner.pdf

[3] [PDF] Design and construction of the Inner Tracker for the CMS Phase-2 https://agenda.infn.it/event/35597/contributions/211610/attachments/111707/159430/Vertex_Talk_final.pdf

[4] PoS(EPS-HEP2023)581; https://inspirehep.net/files/49b9f19722ebe7564be8156ab30f71d6

[5] https://www.epj-conferences.org/articles/epjconf/pdf/2024/05/epjconf_chep2024_02028.pdf

[6] https://arxiv.org/abs/2112.01556

[7] DAQ and Level-1 Track Finding for the CMS HL-LHC Upgrade; https://lss.fnal.gov/archive/2020/conf/fermilab-conf-20-019-e.pdf